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09/833,719	04/13/2001	Takehito Utsunomiya	35.G2774	4977

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EXAMINER	
SINGH, SATWANT K	
ART UNIT	**PAPER NUMBER**
2626	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,719	UTSUNOMIYA, TAKEHITO	
	Examiner	Art Unit	
	Satwant K. Singh	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 7-9, 12, 13, 16-19, 22-24, 27, 28, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishida et al. (US 6,775,245).

3. Regarding Claim 1, Ishida et al disclose an image processing apparatus having a plurality of image processing means for performing predetermined image processing on input image data and for outputting processed image data, said image processing apparatus comprising: creation means for creating packet data by adding to the image data a header in which image processing information is described (Fig. 15) (RAM 80 is divided into a header area and a data area) (col. 9, lines 45-55); and transfer means for transferring the packet data between said creation means and each image processing means (transfer of image data) (1394 provides for asynchronous transfer and isochronous transfer as packet transfer methods) (col. 6, lines 32-36) , wherein said plurality of image processing means inputs the packet data from said transfer means, performs image processing on the image data on a basis of the image processing information described in the header, recreates packet data by adding a header in which

the image processing information is rewritten to the image data after processing, and outputs the recreated packet data to said transfer means (Fig. 1A) (arbitration, packet transfer and acknowledgement) (col. 6, lines 37-48).

4. Regarding Claim 2, Ishida et al disclose an image processing apparatus, wherein said image processing information is processing sequence information of image processing performed by said plurality of image processing means and processing content information of image processing performed by each image processing means (both the print data and the control-related data such as command data and status data are transferred asynchronously) (col. 15, lines 47-55)

5. Regarding Claim 3, Ishida et al disclose an image processing apparatus, wherein identification information of the image processing means and processing content information corresponding to the identification information are described in the header from the beginning thereof in accordance with a sequence in which processing is to be performed (RAM 80 is divided into a header area and a data area) (col. 9, lines 45-55).

6. Regarding Claim 4, Ishida et al disclose an image processing apparatus, wherein said image processing means comprises: input means for inputting the packet data in such a manner as to be divided into a header and image data (RAM 80 is divided into a header area and a data area) (col. 9, lines 45-55); header analysis means for analyzing the processing content information described at the beginning of the header input by said input means (CPU 66 accesses the header area through CPU bus 96) (col. 12, lines 45-51); processing means for performing processing on the image data input by said input means on a basis of an analysis result by said header analysis means (work

area of CPU 66) (col. 13, lines 23-33); header creation means for creating a new header such that identification information of the image processing means which next performs image processing and processing content information corresponding to the identification information are located at the beginning of the header(header is attached to the data in RAM 914) to create a packet that conforms to IEEE 1394. The thus created packet is sent to another node through the path comprising the data transfer control device 932 and the PHY chip 930) (col. 10, lines 35-41); and output means for newly creating packet data from the image data processed by said image processing means and from the header created by said header creation means and for outputting the newly created packet data (CPU bus 96 can be used solely for controlling data transfer) (co. 11, lines 1-8).

7. Regarding Claim 7, Ishida et al disclose an image processing apparatus which has a plurality of image processing means for performing predetermined image processing on input image data and for outputting the image data and which performs a plurality of device function operations in parallel using a connected external device, said image processing apparatus comprising: first creation means for adding to the image data a header in which image processing information is described corresponding to a first device function operation in order to create first packet data (first data pointer); second creation means for adding to the image data a header in which image processing information is described corresponding to a second device function operation in order to create second packet data (second data pointer) (col. 20, lines 58-67, col. 21, lines 1-18); and transfer means for transferring packet data among said first

creation means, said second creation means, and each image processing means (first or second asynchronous transfer) , wherein said plurality of image processing means comprise first image processing means which inputs the first packet data from said transfer means, which performs image processing on image data on a basis of the image processing information described in the header, which creates packet data by adding a header in which the image processing information is rewritten to the image data after processing, and which outputs the packet data to said transfer means (packet assembly circuit 280 reads a header from the header area of the RAM 80 and data form the data area thereof, and assemble a send packet having a frame made up of this header and data) (col. 21, lines 39-56), and second image processing means, while processing related to said first packet data is being performed in said first image processing means, which inputs the second packet data from said transfer means, which performs image processing on image data on a basis of the image processing information described in the header, which creates packet data by adding a header in which the image processing information is rewritten to the image data after processing, and which outputs the packet data to said transfer means (pointer update circuit 284 is a circuit for updating header and data pointers used for reading out headers and data from the ram 80) (col. 21, lines 39-56).

8. Claims 8, 17, and 23 are rejected for the same reason as claim 2.

9. Claims 9, 18, and 24 are rejected for the same reason as claim 3.

10. Regarding Claim 12, Ishida et al disclose an image processing apparatus which is connected to a predetermined data bus and which transfers packet data to and from

an external device via said data bus, the packet data being such that a header in which image processing information is described is added to image data, said image processing apparatus comprising: input means for inputting packet data in such a manner that the data is divided into a header and image data (RAM 80 is divided into a header area and a data area) (col. 9, lines 45-55), to which packet data is added to the header in which identification information of a device and processing content information corresponding to the identification information are described in sequence from a beginning of the header in accordance with a position in the sequence of a device which performs processing (CPU 912 sequentially inputs FIFOs 904 and 906 and sends any packet that are to be transferred) (col. 11, lines 26-30); header analysis means for analyzing processing content information described at the beginning of the header input by said input means (processing of the CPU 66) (col. 13, lines 23-33); image processing means for performing image processing on image data input by said input means on a basis of an analysis result by said header analysis means (Fig. 1A) (arbitration, packet transfer and acknowledgement) (col. 6, lines 37-48); header creation means for creating a new header such that the identification information of an external device which next performs image processing and processing content information corresponding to the identification information are located at the beginning of the header (pointer update circuit 184 increments the header pointer) (col. 20, lines 16-20); and output means for newly creating packet data from the image data processed by said image processing means and from the new header created by said header creation means and for outputting the packet data (DMAC 44 passes a plurality of data pointers,

such as first and second data pointers, to the packet shaping circuit) (co. 20, lines 54-67, col. 21, lines (1-18).

11. Regarding Claim 13, Ishida et al disclose an image processing apparatus, wherein said image processing means performs image processing in a plurality of operation modes, determines an operation mode which is to be performed on a basis of operation mode identification information contained in the analysis result, and performs image processing on the image data (if the RAM 80 is divided into a plurality of areas in this embodiment of the invention, the configuration s=could be such that the size of each area can be controlled variably) (col. 15, lines 60-67, col. 19, lines 1-10).

12. Claim 16 is rejected for the same reason as claim 1.

13. Claim 19 is rejected for the same reason as claim 4.

14. Claim 22 is rejected for the same reason as claim 7.

15. Claim 27 is rejected for the same reason as claim 12.

16. Claim 28 is rejected for the same reason as claim 13.

17. Regarding Claim 31, Ishida et al disclose an image processing apparatus having an image processing unit including N, where N is an integer, function processing sections for performing N different processing functions, and which sequentially transfers a header and image data between the N function processing sections, the header including in sequence first through Nth header parts, each of the N header parts including an ID portion identifying one of the different N processing functions performed by one of the N processing sections, wherein each of said N processing sections comprises: an input device which inputs the header and image data, and separates the

header from the image data (RAM 80 is divided into a header area and a data area) (col. 9, lines 45-55); a header analysis device which identifies which processing function is to be performed based on the ID portion in the first header part of the header (processing of the CPU 66) (col. 13, lines 23-33); a processor which processes the separated image data according to the processing function identified by the ID portion in the first header part of the header as identified by said header analysis device means (Fig. 1A) (arbitration, packet transfer and acknowledgement) (col. 6, lines 37-48); a header creation device which creates a new header from the input header, including in sequence the second through Nth header parts, with the first header part being deleted (pointer update circuit 184 increments the header pointer) (col. 20, lines 16-20); and an output device for combining and outputting the new header and the processed image from said processor for provision to the processing section identified in the second header part of the new header (DMAC 44 passes a plurality of data pointers, such as first and second data pointers, to the packet shaping circuit) (co. 20, lines 54-67, col. 21, lines (1-18).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 5, 14, 20, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al in view of Sato et al (US 6, 810,445).

20. Regarding Claim 5, Ishida et al fails to teach an image processing apparatus, wherein image data which forms the packet data is rectangular image data obtained by dividing image data in page units into rectangular areas of a predetermined size.

Sato et al teach an image processing apparatus, wherein image data which forms the packet data is rectangular image data obtained by dividing image data in page units into rectangular areas of a predetermined size (payload division circuit 250 of Fig 10 divides the transfer data into packets of the payload size the maximum of which is the divisor of the page boundary size) (col. 13, lines 14-20).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Ishida with the teaching of Sato to have the packet data to be page data being sent to the image processor for outputting page information.

21. Claims 14, 20, and 29 are rejected for the same reason as claim 5.

22. Claims 6, 15, 21, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al in view of Pittas et al (US 6, 810,445).

23. Regarding Claim 6, Ishida et al fail to teach an image processing apparatus, wherein image data which forms the packet data is raster image data.

Pittas et al teach an image processing apparatus wherein image data which forms the packet data is raster image data (pixel data is organized in raster format) (col. 5, lines 5-10).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Ishida with the teaching of Pittas to use raster image data to output digital image data.

24. Claims 15, 21, and 30 are rejected for the same reason as claim 6.

25. Claims 10, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al in view of Lenoir (US 6, 741,737).

26. Regarding Claim 10, Ishida et al teach an image processing apparatus wherein said external device comprises a scanner device and a printer device (Figs. 26A, 26B).

Ishida et al fail to teach an image processing apparatus wherein said external device comprises a facsimile device.

Lenoir teaches an image processing apparatus wherein said external device comprises a facsimile device (the conversion of document 30 into the digital image can be done by numerous apparatus including a digital scanner or a facsimile machine) (col. 4, lines 36-48)

Therefore it would have been obvious to one of ordinary skill in the art to have combined the teachings of Ishida with the teaching of Lenoir to also use a facsimile machine to convert a document into a digital image.

27. Claim 25 is rejected for the same reason as claim 10.

28. Claims 11 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al and Lenoir as applied to claims 4 and 25 above, and further in view of Hidaka (US 6,714,312).

29. Regarding Claim 11, Ishida et al and Lenoir fail to teach an image processing apparatus, wherein the device function operations include a copying operation using said scanner device and said facsimile device, and an image communication operation using said facsimile device.

Hidaka teaches an image processing apparatus, wherein the device function operations include a copying operation using said scanner device and said facsimile device, and an image communication operation using said facsimile device (Fig. 10) (scanner module connected to a facsimile line) (col. 11, lines 39-47).
Therefore it would have been obvious to one of ordinary skill in the art to have combined the teachings of Ishida and Lenoir with the teaching of Hidaka to use the copying function of a scanner and the communication operation of a facsimile to convert a document into a digital image.

30. Claim 26 is rejected for the same reason as claim 11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Satwant K. Singh whose telephone number is (703) 306-3430. The examiner can normally be reached on Monday thru Friday 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A. Williams can be reached on (703) 305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satwant Singh

Satwant K. Singh
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sks

MARK WALLERSON
PRIMARY EXAMINER